	Туре	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	9	sato near atsuhiro.in.	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 18:19
2	BRS	L2	11 /1 /5	yamashita near hiroki.in.	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 18:20
3	BRS	L3	475	ozawa near yoshio.in.	US- PGPUB; USPAT;	2005/01/1 1 18:49

	Туре	L	#	Hits	Search Text	DBs	Time Stamp
4	BRS	L4		307	438/294.ccls.	14 D() •	2005/01/1 1 18:52
5	BRS	L6		4	(inter-electrode near dielectric) near15 (isolat\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 18:54
6	BRS	L7		4	(inter near electrode near dielectric) near15 (isolat\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 18:54

	Туре	L i	Hits	Search Text	DBs	Time Stamp
7	BRS	L5	155	(inter-electrode near dielectric)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:00
8	BRS	L8	4283	(silicon near oxide or sio) near15 (dielectric near constant)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:01
9	BRS	L10	2	((silicon near oxide or sio) near15 (dielectric near constant)) near15 (inter-electrode\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:02

	Туре	L	#	Hits	Search Text	DBs	Time Stamp
10	BRS	L11	L	2	((silicon near oxide or sio) near15 (dielectric near constant)) near15 (inter near	IH: P() •	2005/01/1 1 19:02
11	BRS	L9		247	constant)) near15 (electrode\$1)	IH: P() *	2005/01/1 1 19:15
12	BRS	L12	2	59	((silicon near oxide or sio) near15 (dielectric near constant)) near15 (ono)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:06

	Туре	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L13	38	or sio) near15 (dielectric near constant)) near15 (memory near cell)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:06
14	BRS	L14	94	<pre>((silicon near oxide or sio) near15 (dielectric near constant)) near15 (conducti\$3)</pre>	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 1 19:27
15	BRS	L15	2	or sio) near15 (dielectric near constant)) near15 (row or column)	EPO;	2005/01/1 1 19 : 28

	U	1	Document ID	Title	Current OR
1	Χ		US 20050003619	Nonvolatile semiconductor memory and manufacturing method for the same	438/294
2	Χ		US 20050002231	Nonvolatile semiconductor memory and manufacturing method for the same	365/185.01
3	X			Process flow for a performance enhanced MOSFET with self-aligned, recessed channel	438/197
4	Х		US 5792689 A	Double crown capacitor formation for use in DRAM - gives self alignment to node contacts and uses single photoresist masking step	1